CLAIMS

What is claimed is:

1. A method for processing cache memory accesses in a computing system having a requester to submit memory access addresses for requested data, and having a tag memory to store tag addresses corresponding to addresses stored in the cache memory, the method comprising:

retrieving a stored tag address from the tag memory in response to the requester submitting a memory access address;

performing a first comparison of the memory access address to the stored tag address to determine whether the requested data is stored in the cache memory;

monitoring for errors in the stored tag address, wherein the monitoring is performed contemporaneously with the first comparison of the memory access address and the stored tag address;

if a tag address error is detected, disregarding the first comparison, correcting the tag address error, and performing a second comparison of the memory access address and the corrected tag address to determine whether the requested data is stored in the cache memory; and

if no tag address error is detected, utilizing results of the first comparison to determine whether the requested data is stored in the cache memory.

2. The method of Claim 1, wherein monitoring for errors comprises storing a single error correction code with the data stored in the tag memory.

3. The method of Claim 2, wherein the single error ~~correction code~~ is coded to provide error detection for the ~~stored~~ tag address and a plurality of ~~configuration~~ fields.

4. ~~The method of Claim 1, wherein the first comparison compares only~~ the stored tag address with the ~~memory access address~~, and disregards ~~comparison of any~~ stored error correction code bits.

5. The method of Claim 1, wherein the second comparison compares only the stored tag address with the memory address access, and disregards comparison of any stored error correction code bits.

6. The method of Claim 1, wherein performing the first comparison and monitoring for errors in the stored tag address occur contemporaneously with correcting the tag address error and performing the second comparison.

7. The method of Claim 1, wherein correcting the tag address error and performing the second comparison are initiated upon recognition of a tag address error.

8. The method of Claim 1, wherein disregarding the first comparison comprises blocking passage of the results of the first comparison through an output gate.

9. The method of Claim 8, wherein blocking passage of the first comparison results comprises:

providing an error signal to the output gate when a tag address error is detected; and

disabling an output of the output gate upon receipt of the error signal.

10. The method of Claim 9, further comprising enabling the tag address error to be corrected and the second comparison of the memory access and corrected tag addresses to be performed in response to the error signal.

11. A cache hit detector, comprising:

(a) a tag memory to store tag addresses corresponding to addresses currently cached;

(b) a fast hit detection circuit, comprising:

(i) a first address compare module coupled to the tag memory to receive a tag address and to compare the tag address to a requested address;

(ii) an error detector coupled to the tag memory to receive the tag address and to determine whether there are any errors in the tag address;

(iii) a gated output module coupled to the first address compare module and the error detector to output a fast hit indication if and only if no error is discovered by the error detector and the requested address is stored in the tag memory;

(c) a slow hit detection circuit, comprising:

(i) an error correction circuit coupled to the tag memory to receive the tag address and to correct errors in the tag address; and

(ii) a second address compare module coupled to the error correction circuit to receive the corrected tag address and to compare the corrected tag address to a current address.

12. The cache hit detector as in Claim 11, wherein the fast hit detection circuit and the slow hit detection circuit are coupled in parallel such that the first address compare module and the error detector perform operations concurrently with operations of the second address compare module and the error correction circuit.

13. The cache hit detector as in Claim 11, further comprising latching means to coordinate timing between the fast hit detection circuit and the slow hit detection circuit.

14. The cache hit detector as in Claim 11, wherein the tag memory further stores an error correction code for each block of data stored in the tag memory, wherein each block of data is associated with a single error correction code, and the single error correction code provides error correction capabilities for the stored tag address and a plurality of configuration fields.

15. The cache hit detector as in Claim 11, wherein the first address compare module and the error detector are coupled in parallel to contemporaneously compare the tag address to a requested address and determine whether there are any errors in the tag address.

16. The cache hit detector as in Claim 11, further comprising:

a first latch coupled to the first address compare module to latch comparison results;

a second latch coupled to the error detector to latch a resulting error indicator signal; and

wherein the comparison results and the error indicator signal are not passed to the gated output until both the comparison results and the error indicator signal are available at the first and second latches, and until

simultaneously clocked to concurrently provide the comparison results and the error indicator signal to the gated output.

17. The cache hit detector as in Claim 11, wherein the error detector determines whether there are any single bit errors in the tag address.

18. A data processing system comprising:

(a) a main memory module for storing data;

(b) at least one cache memory coupled to the main memory module to cache at least a portion of the data stored in the main memory module;

(c) at least one processing unit to process data and to control data access with the main memory module and the cache memory, the processing unit comprising:

(1) a tag memory to store tag addresses corresponding to addresses currently cached;

(2) a fast hit detection circuit, comprising:

(i) a first address compare module coupled to the tag memory to receive a tag address and to compare the tag address to a requested address;

(ii) an error detector coupled to the tag memory to receive the tag address and to determine whether there are any errors in the tag address;

(iii) a gated output module coupled to the first address compare module and the error detector to output a fast hit indication if and only if no error is discovered by the error detector and the requested address is stored in the tag memory;

(3) a slow hit detection circuit, comprising:

(i) an error correction circuit coupled to the tag memory to receive the tag address and to correct errors in the tag address; and

(ii) a second address compare module coupled to the error correction circuit to receive the corrected tag address and to compare the corrected tag address to a current address.

19. The data processing system of Claim 18, wherein the fast hit detection circuit and the slow hit detection circuit are configured in parallel such that the first address compare module and the error detector perform operations concurrently with operations of the second address compare module and the error correction circuit.

20. The data processing system of Claim 18, wherein the tag memory further stores an error correction code associated with each block of data, wherein each block of data is associated with a single error correction code, and the single error correction code provides error correction capabilities for the stored tag address and a plurality of configuration fields.

21. A cache hit detector, comprising:

(a) means for storing tag memory addresses corresponding to addresses of data currently stored in cache memory;

(b) means for providing alternate cache hit detection via concurrent processing on each of at least two cache hit detection paths, the alternate cache hit detection means comprising:

(1) first hit detection path means for detecting cache hits without first performing error detection and correction;

(2) second hit detection path means for detecting cache hits, the second hit detection path means comprising:

(i) means for detecting errors in the tag memory address;

(ii) means for correcting the tag memory address if errors in the tag memory address are discovered;

(iii) means for detecting for cache hits using the corrected tag memory address if errors in the tag memory address are discovered; and

(iv) means for disabling the first hit detection path means if errors in the tag memory address are discovered.

22. The cache hit detector as in Claim 21, further comprising means for coordinating timing between the first hit detection path means and the second hit detection path means.